MC20901
D-PHY 5-Channel Slave Receiver Evaluation Board User's Guide

PRELIMINARY DATASHEET

Version 1.00

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Meticom GmbH

Revision History

MC20901		
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1 Introduction

This document describes the FPGA Mezzanine Card (FMC) MC20901 Slave Receiver Evaluation Board (MC20901-EVB) from Meticom GmbH. The MC20901-EVB implements a 5 channel D-PHY Slave Receiver which enables the reception of a MIPI D-PHY compliant data stream. The D-PHY Slave Interface is implemented using the Meticom's MC20901 high performance FPGA bridge IC. The MC20901 is a five channel device which converts a MIPI D-PHY compliant input stream into LVDS (high speed) and CMOS (low speed) output data streams.

2 Features

- MIPI D-PHY Slave Receiver input interface via SMA connectors
- 5x D-PHY Slave Receiver Channels (4 data plus 1 clock)
- Bi-directional communication (LP mode only) using Bus Turnaround (BTA) on EVB CH3
- I2C connector for CSI-2 applications
- Board schematics, design files and a bill of materials are available.

3 System Setup

Hardware

The table below details the board validated to support the MC20901-EVB. The ML605 board provides one FMC high pin count (HPC) (J64) and one FMC low pin count (LPC) (J63) connector interface. The MC20901-EVB connector is compatible with the HPC or LPC connector of the Xilinx Virtex-6 FPGA ML605 Evaluation Kit. However, if using the supplied FPGA software the MC20901-EVB connector must be installed on the HPC J64 connector of the ML605.

Xilinx Platform	Part Number	FMC HPC Connector	FMC LPC Connector
Virtex-6 FPGA ML605 Evaluation Kit	EK-V6-ML605-G	J64	J63

Table 1: MC20901-EVB Supported Boards

Software

Example designs that use this hardware are discussed in a separate document.

Board Installation

Complete the following steps to install the MC20901-EVB to a Xilinx board. For additional information on Xilinx boards, refer to the particular board's user guide.

1. Turn off the ML605 board's DC power switch and disconnect its input power source.
2. Remove the MC20901-EVB from the electrostatic device (ESD) bag.
3. Using a small screwdriver, remove the two screws from the bottom side of the two standoffs on the MC20901-EVB.
4. Install the The MC20901-EVB to the ML605 FMC HPC connector J64.
5. Turn the ML605 and attached MC20901-EVB board over such that the ML605 FPGA is facing the table. Install two screws from the bottom side of ML605 board's FMC HPC mounting holes into the two standoffs attached to the MC20901-EVB. Hand tighten the two mounting screws to the bottom of the board.
6. Turn the ML605 and attached MC20901-EVB boards over such that the Xilinx FPGA is visible.
7. Connect the input power source to the ML605 board. Turn the ML605 board power input switch to ON.

The system is now ready for use.

4 Board Technical Description

The MC20901-EVB is populated with an FMC HPC connector which enables it to be plugged into the Xilinx Virtex-6 ML605 evaluation board. The Virtex-6 FPGA controls the D-PHY operation of the board via this FMC connector.

The MC20901-EVB module architecture is detailed in the following block diagram.

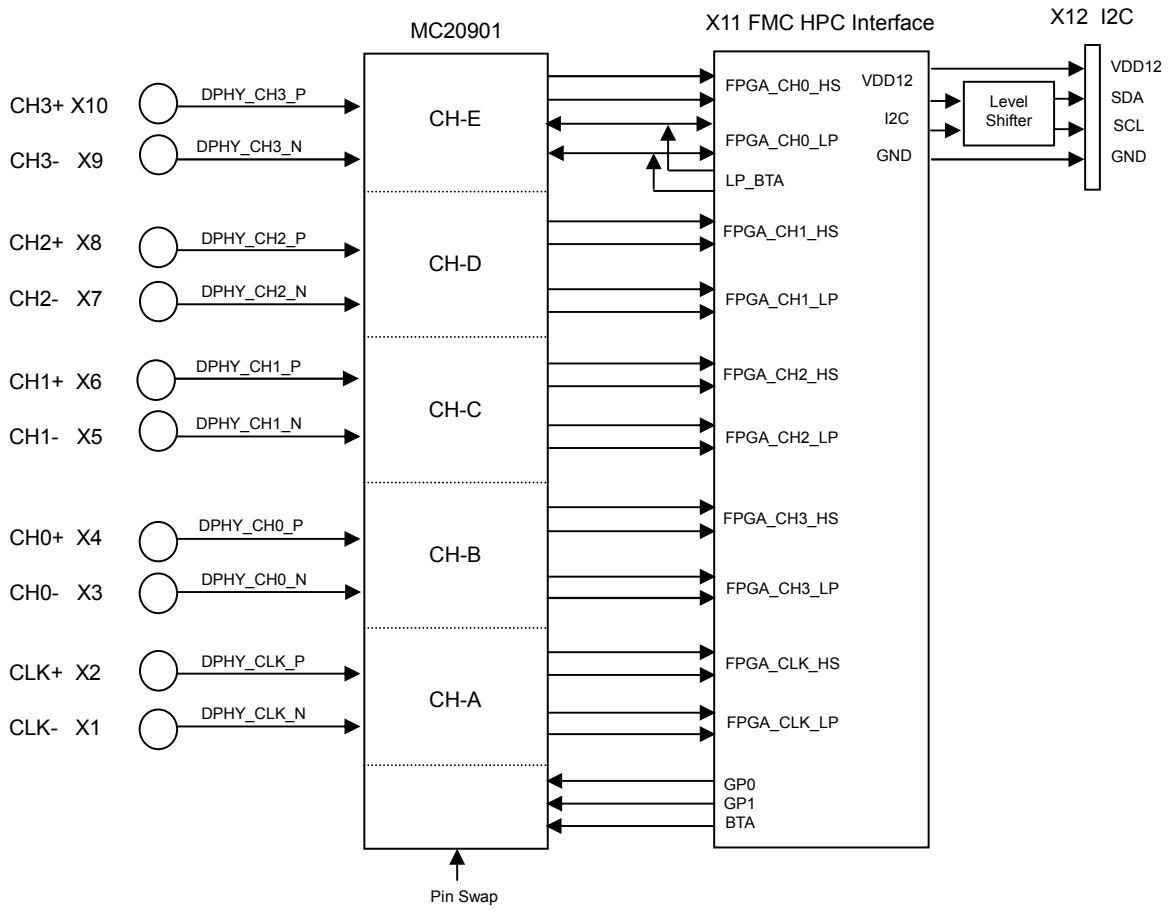

Figure 1: MC20901-EVB Block Diagram

Notice:
Bus Turnaround functionality is provided on FPGA channel 0 (LP mode Only) which corresponds to Channel E (CH-E) of the MC20901 , CH3 of the MC20901-EVB.
The MC20901 provides a Bus Turnaround functionality also on Channel A. Please note, that in Figure 1 the clock signal is connected to Channel A. I this special case it is not possible to use Bus Turnaround on Channel A.

The MC20901 is configured via the FMC GP1:GP0 outputs, there are four possible combinations as listed in the table below. The output pins are directly driven from the FPGA outputs. The MC20901-EVB utilities Channel E of the MC20901 for Bus Turnaround therefore GPO1:GPO0 = 10 “Channel E Select”

GPIO-1	GPIO-0	Description
0	0	IC Power Down
0	1	LVDS to SLVS Level Shift
1	0	Bus Turnaround valid on channel E (default setting by solder jumper on the rear. SJ1, SJ2)
1	1	Bus Turnaround valid on channel A

Table 2: MC20901 GPIO Configuration

There is a solder jumper configuration option on the rear of the EVB to provide a fixed configuration. If there is requirement to control the configuration by FPGA please first remove the solder jumper on the rear. Otherwise the FPGA output will be shorten.

Bus turnaround enables FPGA_CH0 to have bidirectional capability in (Low Power) LP Mode.
The Bus Turnaround feature uses a half-duplex configuration, this requires a method of placing FPGA_CH0 in Forward (TX) or Reverse (RX) direction. The BTA input of the MC20901 is used for this purpose and is controlled via the “BTA” pin from the FMC connector. If BTA = '0' then the Receive (RX) direction is active, if BTA = '1' then the Slave Transmit (TX) direction is active.

BTA	Description
0	Bus Turnaround not active (Slave RX Mode)
1	Bus Turnaround active (Slave TX Mode)

Table 3: MC20901-EVB BTA

Pin Swap configuration is described in the table below:

PINSWAP	Description
0	Pin Swap off (default setting by solder jumper on the rear; SJ5)
1	Pin Swap D-PHY-X (swaps D-PHY-X-P and D-PHY-X-N pins)
Floating	Pin Swap HS-X (swaps HS-X-P and HS-X-N pins)

Table 4: MC20901-EVB PINSWAP

For more detailed information regarding device configuration and connection options please refer to the MC20901 datasheets.

A 4-way pin header (X12) provides the option for an external I2C interface with a +12V dc supply pin. This provides the possibility to control I2C based peripherals on the D-PHY slave side. The I2C signals are generated by the FPGA. A level shifter IC (TXS0102) on the board converts the 2.5 V I2C outputs from the FPGA into 3.3V level outputs which can then be connected to an I2C peripheral.

FMC Connector

The FMC connector (X11) is the Samtec FMC LPC connector ASP-134640-01. It provides the main control and data connections to the Meticom MC20901 bridge IC, the external I2C bus SDA and SCL connections and the associated DC supply voltage. The FMC pin allocation for the MC20901-EVB is defined in the following tables.

Note, that the direction of the pins for the FMC connector are given with respect to the FPGA direction, i.e. an output is an FPGA configured output pin.
See the Xilinx board user guides and schematics for a description of the features provided by the FMC connector interfaces such as FPGA bank connectivity and FPGA pin assignments.

Pin	Net Name	I/O	Description
C1, C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, C24, C25, C28, C29, C32, C33, C36, C38, C40	GND		Ground
C2, C3, C6, C7, C10, C11, C26, C27, C30, C31, C34	-		No Connection
C35, C37	VDD12	O	12V Positive Supply
C39	VDD3V3	O	3.3V Positive Supply
C14	FPGA_CH3_HS_P	I	D-PHY HS RX Data Lane 3P LVDS
C15	FPGA_CH3_HS_N	I	D-PHY HS RX Data Lane 3N LVDS
C18	FPGA_CH3_LP_P	I	D-PHY LP RX Data Lane 3P CMOS 2.5V
C19	FPGA_CH3_LP_N	I	D-PHY LP RX Data Lane 3N CMOS 2.5V
C22	I2C_SCL_2V5	O	I2C SCL CMOS 2.5V
C23	I2C_SDA_2V5	I/O	I2C SDA CMOS 2.5V

Table 5: FMC Connector Row C Pin Allocation

Pin	Net Name	I/O	Description
D4, D5, D8, D9, D11, D12, D20, D21, D23, D24, D26, D27, D29, D30, D31, D32, D33, D34, D35, D37, D39	-		No Connection
D2, D3, D6, D7, D10, D13, D16, D19, D22, D25, D28	GND		Ground
D36, D38, D40	VDD3V3	O	+3.3V Positive Supply
D14	FPGA_CH2_HS_P	I	D-PHY HS RX Data Lane 2P LVDS
D15	FPGA_CH2_HS_N	I	D-PHY HS RX Data Lane 2N LVDS
D17	FPGA_CH1_LP_P	I	Positive low speed CMOS input to FPGA for D-PHY data lane 1
D18	FPGA_CH1_LP_N	I	Negative low speed CMOS input to FPGA for D-PHY data lane 1
D1	EN_PWR	O	Supply voltage control pin (not applicable) (default setting by solder jumper on the rear is “on” SJ6, SJ7)

Table 6: FMC Connector Row D Pin Allocation

Pin	Net Name	I/O	Description
G1, G4, G5, G8, G11, G14, G17, G20, G23, G26, G29, G32, G35, G38, G40	GND		Ground
G2, G3, G12, G13,G21, G22, G24, G25, G27, G28, G30, G31, G33, G34, G36, G37	-		No Connection
G39	VDD25	O	+2.5V Positive Supply
G6	FPGA_CLK_HS_P	I	D-PHY HS Clock Lane CLK_P LVDS
G7	FPGA_CLK_HS_N	I	D-PHY HS Clock Lane CLK_N LVDS
G9	FPGA_CH0_LP_P	I	D-PHY LP RX Data Lane 0P CMOS 2.5V
G10	FPGA_CH0_LP_N	I	D-PHY LP RX Data Lane 0N CMOS 2.5V
G15	FPGA_CH1_HS_P	I	D-PHY HS RX Data Lane 1P LVDS
G16	FPGA_CH1_HS_N	I	D-PHY HS RX Data Lane 1N LVDS
G18	FPGA_CH2_LP_P	I	D-PHY LP RX Data Lane 2P CMOS 2.5V
G19	FPGA_CH2_LP_N	I	D-PHY LP RX Data Lane 2N CMOS 2.5V

Table 7: FMC Connector Row G Pin Allocation

Pin	Net Name	I/O	Description
H1	-		Ground via resistor
H2, H4, H5, H7, H8, H14, H22, H23, H25, H26, H28, H29, H31, H32, H34, H35	-		No Connection
H3, H6, H9, H12, H15, H18, H21, H24, H27, H30, H33, H36, H39	GND		Ground
H40	VDD25	O	+2.5V Positive Supply
H10	FPGA_CLK_LP_P	I	D-PHY LP Clock Lane P CMOS 2.5V
H11	FPGA_CLK_LP_N	I	D-PHY LP Clock Lane N CMOS 2.5V
H13	BTA	O	BTA '0' = RX Path Selected '1' = TX Path Selected (Bus Turnaround) CMOS 2.5V
H16	FPGA_CH0_HS_P	I	D-PHY HS Data Lane 0P LVDS
H17	FPGA_CH0_HS_N	I	D-PHY HS Data Lane 0N LVDS
H19	LP_BTA_P	O	D-PHY LP Data Lane 0P CMOS 2.5V
H20	LP_BTA_N	O	D-PHY LP Data Lane 0N CMOS 2.5V
H37	GPIO_1	O	Configuration GPIO-1 Default mode = '1' (by solder jumper) CMOS 2.5V
H38	GPIO_0	O	Configuration GPIO-0 Default mode = '0' (by solder jumper) CMOS 2.5V

Table 8: FMC Connector Row H Pin Allocation

SMA Connectors

The SMA connectors supply the D-PHY Master compliant signals and can be directly connect to a D-PHY Master device, for example a CSI-2 Camera or the Meticom MC20902-EVB Master Transmitter evaluation board.

The MC20901-EVB SMA connectors are labelled X1 through X10:

SMA Connector	Name	I/O	Description
X10	CH3+	I/O	D-PHY Data Lane 3P
X9	CH3-	I/0	D-PHY Data Lane 3N
X8	CH2+	I	D-PHY Data Lane 2P
X7	CH2-	I	D-PHY Data Lane 2N
X6	CH1+	I	D-PHY Data Lane 1P
X5	CH1-	I	D-PHY Data Lane 1N
X4	CH0+	I	D-PHY Data Lane 0P
X3	CH0-	I	D-PHY Data Lane 0N
X2	CLK+	I	D-PHY Clock Lane P
X1	CLK-	I	D-PHY Clock Lane N

Table 9: D-PHY S-RX SMA Connectors

I2C Connector

The I2C connection to the FPGA is available on connector X12.
Note there are no pull-up resistors on the SDA or SCL lines, it is assumed that these are provided on the I2C bus slave side.

Pin	Name	Description
1 (Square)	VDD12	12V supply from FPGA board
2	SDA	I2C Data (3.3V level)
3	SCL	I2C Clock (3.3V level)
4	GND	Ground

Table 10: I2C Connector

5 Known Issues & Limitations

I2C pull-up resistors

There are no pull-up resistor provide on the I2C SDA or SCL lines.

6 Additional Documentation

To make best use of MC20901-EVB it is recommended that the user is familiar with the following resources:

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8 Contact Information

Meticom GmbH

Suedfeld 12
30989 Gehrden
Germany

Tel: +49 5108 918640
Fax: +49 5108 918640

www.meticom.com