MC20001

FPGA Bridge IC

for

MIPI D-PHY Systems
and
SLVS to LVDS Conversion

DATASHEET

Version 1.09

August 2016

Meticom GmbH

Revision History

MC20001		
Version	**Date of Issue**	**Change**
1.01	April 25, 2012	• First Draft
1.02	May 10, 2012	• Updated maximum speed • Added application examples • Added new configuration option
1.03	August 10, 2012	• Updated AC characteristics
1.04	September 17, 2012	• Updated DC characteristics (Table 3)
1.05	November 22, 2012	• Added thermal pad dimensions and description • Added RoHS statement
1.06	December 20, 2012	• Table 2: V_{SS} renamed to GND
1.07	August 19, 2013	• Table 3: Voltage ranges adapted for V_{CM-IN} and $\|V_{IN-Diff}\|$ • Table 4: definitions corrected and values updated
1.08	April 4, 2014	• Package drawing update • Application note added - input to output signal diagram
1.09	August 1, 2016	• Chapter 6.6 Figure number corrected • Figure 8: Signal name error corrected • 'Preliminary' status of data sheet removed

Table of Contents

1 General Description

The MC20001 is a high performance FPGA bridge IC, which converts a single MIPI D-PHY compliant input stream into LVDS high speed and CMOS low speed output data streams.
The MC20001 can also convert an SLVS signal into an LVDS signal.

The MC20001 outputs can be directly connected to FPGAs or DSPs.

Data rates can be from 0 Mbps to 2.5 Gbps in HS (High Speed) mode and up to 20 Mbps in LPDT (Low Power Data Transmission) mode.

2 Key Features

- Input is compliant to MIPI D-PHY interfaces using the DSI, CSI-1 and CSI-2 standards
    - HS mode data rate: up to a maximum of 2.5 Gbps
    - LPDT mode data rate: up to 20 Mbps
- Conversion of SLVS input to LVDS output
    - SLVS data rate: up to a maximum of 2.5 Gbps
- D-PHY termination automatically switched depending on HS or LP mode
- No additional level shifters needed
- Arbitrary power up sequence
- Available as a bare die
    - RoHS compliant, Pb-free
- Available in a TQLMP-16 package
    - 3mm * 3mm * 0.75mm
    - 0.5mm pitch
    - RoHS compliant, Pb-free

3 Block Diagram

3.1 Block Diagram

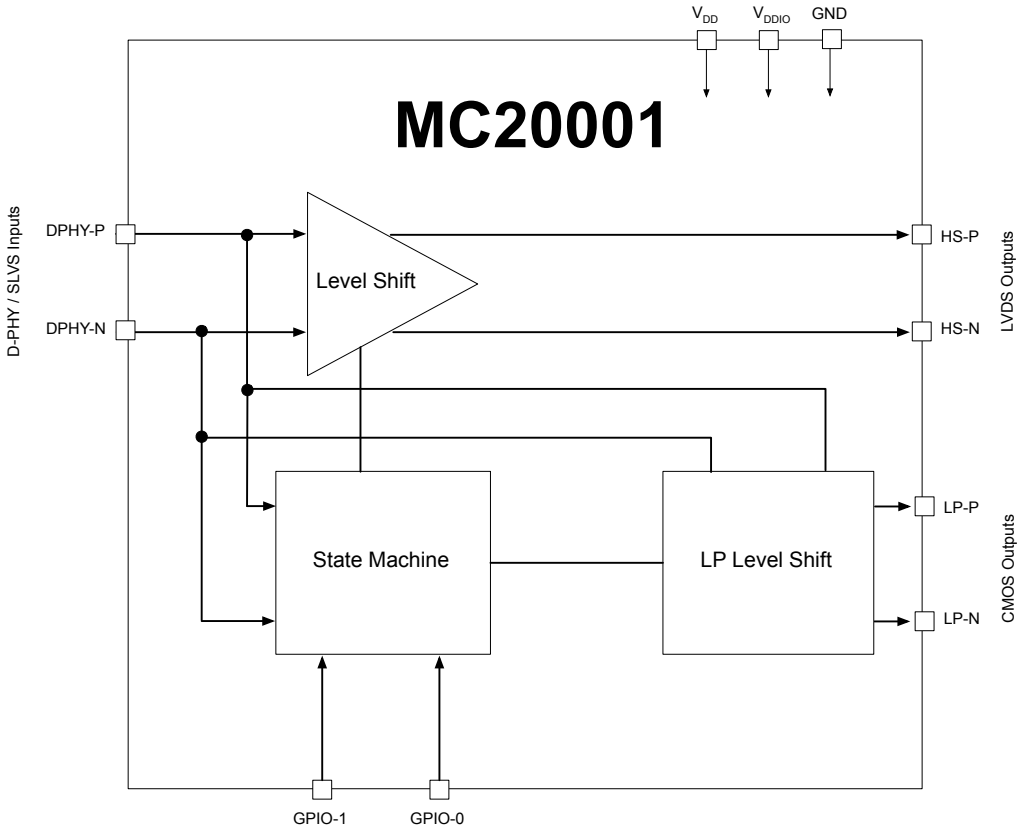


Figure 1: Functional Block Diagram of the MC20001

4 Parametrics

4.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{DDIO}	Supply voltage		-0.5	3.6	V
V_{DD}	Supply voltage		-0.5	2.0	V
T_{STG}	Storage temperature		-55	125	°C
T_J	Junction temperature		-55	125	°C
V_{ESD}	Electrostatic discharge voltage capability	(HBM; 100 pF, 1.5 kΩ)	2.0		kV
$V_{ESD\text{-}Dout}$	Electrostatic discharge voltage capability at differential I/Os	(HBM; 100 pF, 1.5 kΩ)	500		V

Table 1: Absolute Maximum Ratings

Notes:

Absolute Maximum Ratings may not be exceeded to the device without causing permanent damage or degradation. Exposures to these values for extended periods may affect device reliability. If the device is operated beyond the range of Operating Conditions functionality is not guaranteed.

4.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDIO}	Supply voltage		2.3	2.5	2.7	V
V_{DD}	Supply voltage		1.1	1.2	1.3	V
GND	Ground			0		V
$V_{noise,VDD}$	Maximum allowed supply noise on V_{DD}	see Figure 2			100	mV_{pp}
T_A	Ambient temperature		-40	25	100	ºC

Table 2: Operating Conditions

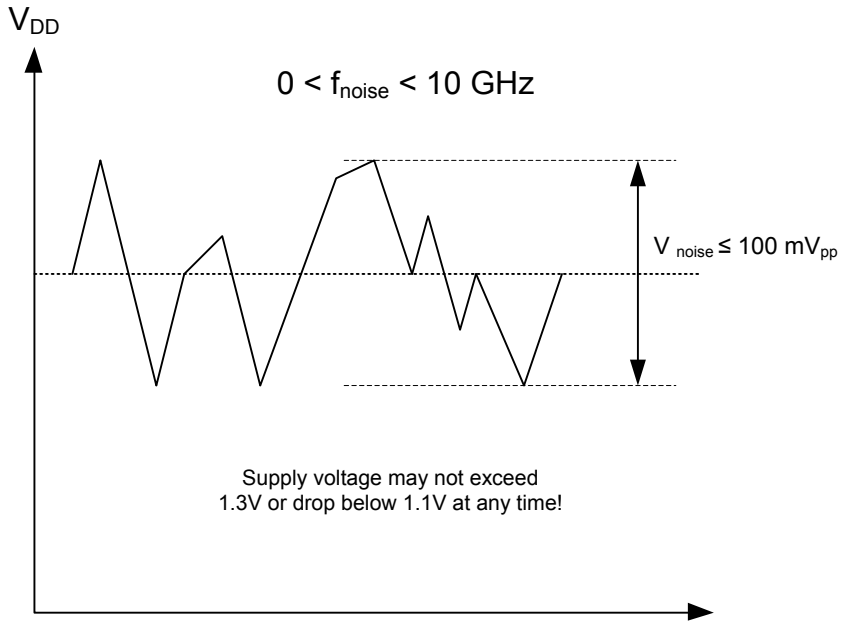


Figure 2: Maximum Allowed Supply Noise on V_{DD}

4.3 DC Characteristics

(At recommended operating conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD25HS}	HS mode supply current VDDIO	@2.5Gbps	5.5	6.7	8	mA
I_{DD12HS}	HS mode supply current VDD	@2.5Gbps LP-P, LP-N constant low state	200	260	320	uA
I_{DD25LP}	LP mode supply current VDDIO	@20Mbps HS-P HS-N constant logical low *1	5.5	6.7	8	mA
I_{DD12LP}	LP mode supply current VDD	@20Mbps	120	250	400	uA
Single Ended Outputs (LP-P, LP-N)						
V_{OH}	LP high level output voltage	Tracks VDDIO	2.3	2.5	2.7	V
V_{OL}	LP low level output voltage			0	0.2	V
Single Ended Inputs (GPIO-0, GPIO-1)						
V_{IH}	GPIO high level input voltage		0.7		VDDIO	V
V_{IL}	GPIO low level input voltage		0		0.2	V
HS Outputs (HS-P, HS-N)						
V_{CM-OUT}	Output common mode voltage	Tracks VDD	1.09	1.2	1.31	V
$\|V_{DO-Diff}\|$	Differential output voltage		260	300	350	mVp
Z_{OD}	Output impedance	Differential	80	100	120	Ω
D-PHY Inputs (D_{PHY-P}, D_{PHY-N})						
V_{IH}	LP high level input voltage		0.88		1.35	V
V_{IL}	LP low level input voltage		0		0.55	V
I_{IH}	High level Input current	Input termination off			100	nA
I_{IL}	Low level input current	Input termination off			100	nA
C_{IN}	Input capacitance	Including package		1	1.5	pF
V_{CM-IN}			70	200	330	mV
$\|V_{IN-Diff}\|$		@ up to 1.5Gbps	70	200	400	mV
		@ above 1.5Gbps	140	200	400	mV
Z_{IN}		Differential	80	100	120	Ω

*1 20pF load cap on LP-N, LP-P

Table 3: DC Characteristics

4.4 AC Characteristics

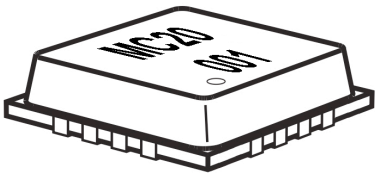
(At recommended operating conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
t_{PU}	Power up time				10	µs	
t_{HS}	Min delay HS sequence to HS data				2	ns	
Single Ended Outputs (LP-P, LP-N)							
BR_{LP}	Maximum LP output bit rate		20			Mbps	
HS Outputs (HS-P, HS-N)							
BR_{HS}	Maximum supported output bit rate		2.5			Gbps	
T_r/T_f	Output data transition time	20%-80%		90	140	ps	
T_{DEL}	Propagation delay		300	500	900	ps	
S_{22}	Output return loss	@ 500 MHz			15	dB	
J_D	Deterministic output jitter				30	ps	
J_R	Generated random jitter			0.35	0.7	ps_{rms}	
J_{PSRR}	Jitter caused by PSRR	Supply noise @ VDD		1	2	ps/mV	
Differential Inputs (D_{PHY-P}, D_{PHY-N})							
BR_{HS}	Maximum supported input bit rate		2.5			Gbps	
S_{11}	Input return loss	@ 500 MHz			15	dB	

Table 4: AC Characteristics

5 Package Information

5.1 TQLMP-16 Package



(drawing not to scale)

- Package Type: Thin Quad Leadless Molded Package (TQLMP)
- Package Dimensions: 3.0 x 3.0 x 0.75 mm³
- Pin Pitch: 0.5 mm

5.2 Pin Description

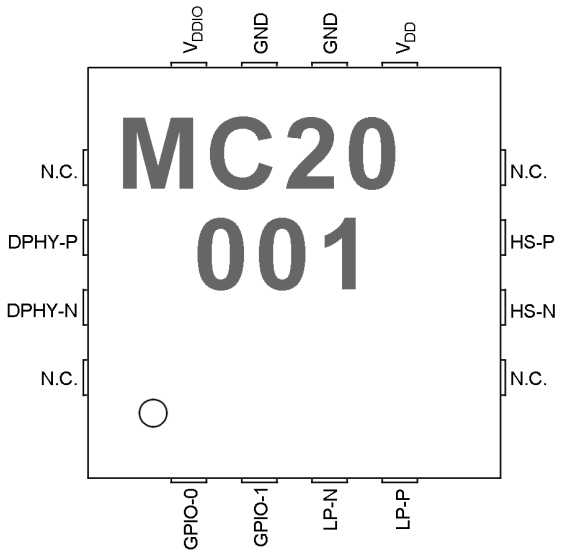
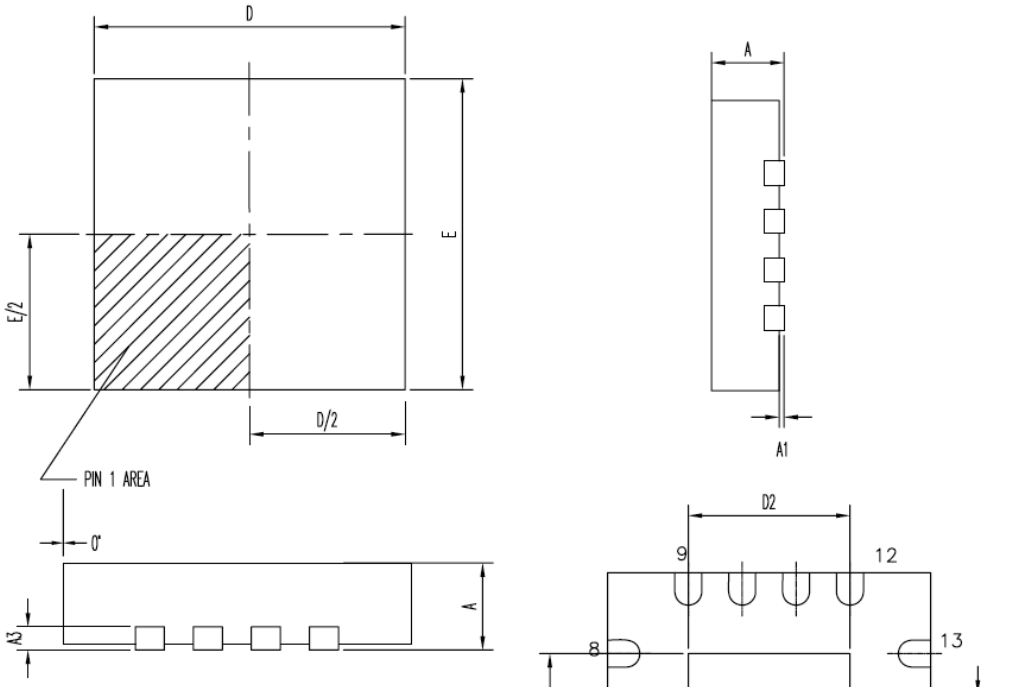


Figure 3: Pin Assignment MC20001

Pin Name	Pin No.	I/O	Type	Description
VDDIO	12	I	Supply	Supply voltage for the LVDS output stage and internal level shifters
VDD	9	I	Supply	Supply voltage for the SLVS input driver and internal logic
GND	10, 11	-	-	Global ground
HS-P	7	O	LVDS	Positive LVDS high speed output
HS-N	6	O	LVDS	Negative LVDS high speed output
LP-P	4	O	CMOS	Positive CMOS low power data output
LP-N	3	O	CMOS	Negative CMOS low power data output
GPIO-0	1	I	CMOS	General purpose configuration input 0
GPIO-1	2	I	CMOS	General purpose configuration input 1
DPHY-P	14	I	SLVS/CMOS	MIPI D-PHY compliant positive input or SLVS positive input
DPHY-N	15	I	SLVS/CMOS	MIPI D-PHY compliant negative input or SLVS negative input
N.C.	5, 8, 13, 16	-	-	Do not connect
Thermal Pad		-	-	Thermal Pad may be connected to GND or left floating (n.c.)

Table 5: Pin Description

5.3 Package Information



JEDEC#	MO-220J			
TYPE	16 TQLMP			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.7	0.8	27.56	31.50
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	2.9	3.1	114.17	122.05
E	2.9	3.1	114.17	122.05
D2	1.4	1.6	55.12	62.99
E2	1.4	1.6	55.12	62.99
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.25	0.35	9.84	13.78
θ°	0°	4°	0°	4°
ND	4			
NE	4			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

Figure 4: Mechanical Dimensions TQLMP-16

6 Application Notes

6.1 Application Overview

MC20001 can be used together with D-PHY source (such as a camera) as shown. It can take the D-PHY compliant source signals from the camera and convert them into standard LVDS and CMOS signals, which can then be fed directly into an FPGA for analysis and processing.

The diagram also shows the MC20002, which performs the reverse function of the MC20001.

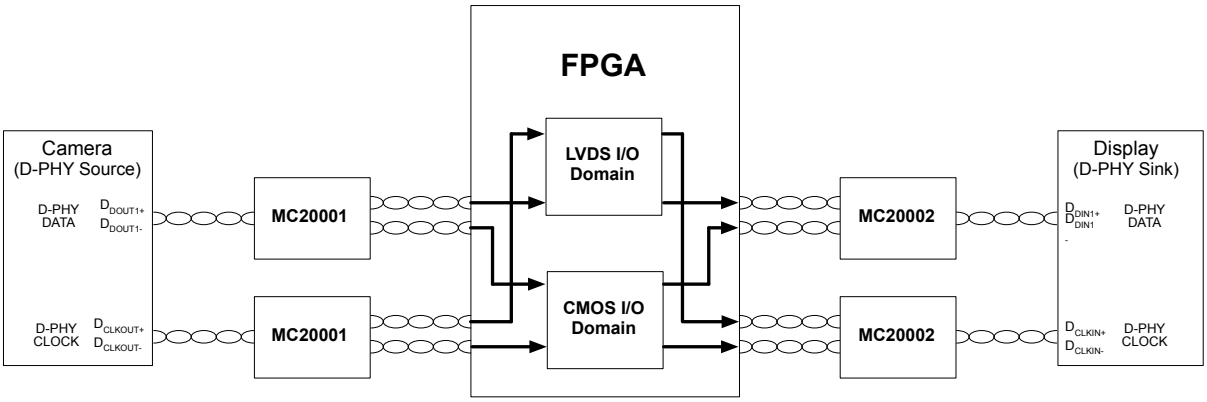


Figure 5: Application Diagram

6.2 D-PHY to FPGA Bridge Application

In this example one D-PHY clock lane and one D-PHY data lane are shown. Additional D-PHY data lanes can be implemented in the same way.

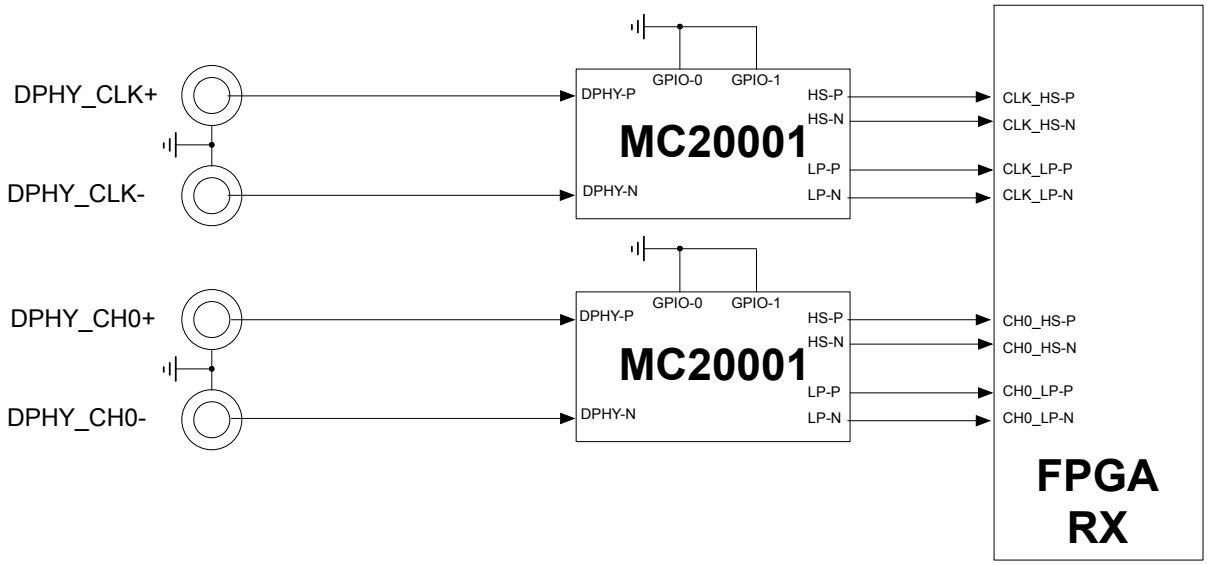


Figure 6: D-PHY to FPGA Bridge Application

6.3 D-PHY to FPGA Bridge Application with Bus Turnaround

In this example one D-PHY clock lane and one D-PHY data lane are shown. The D-PHY data lane uses an MC20002 to implement the bus turnaround (BTA) function. Additional D-PHY data lanes, which do not use BTA, can be implemented in the same way as the D-PHY clock lane.

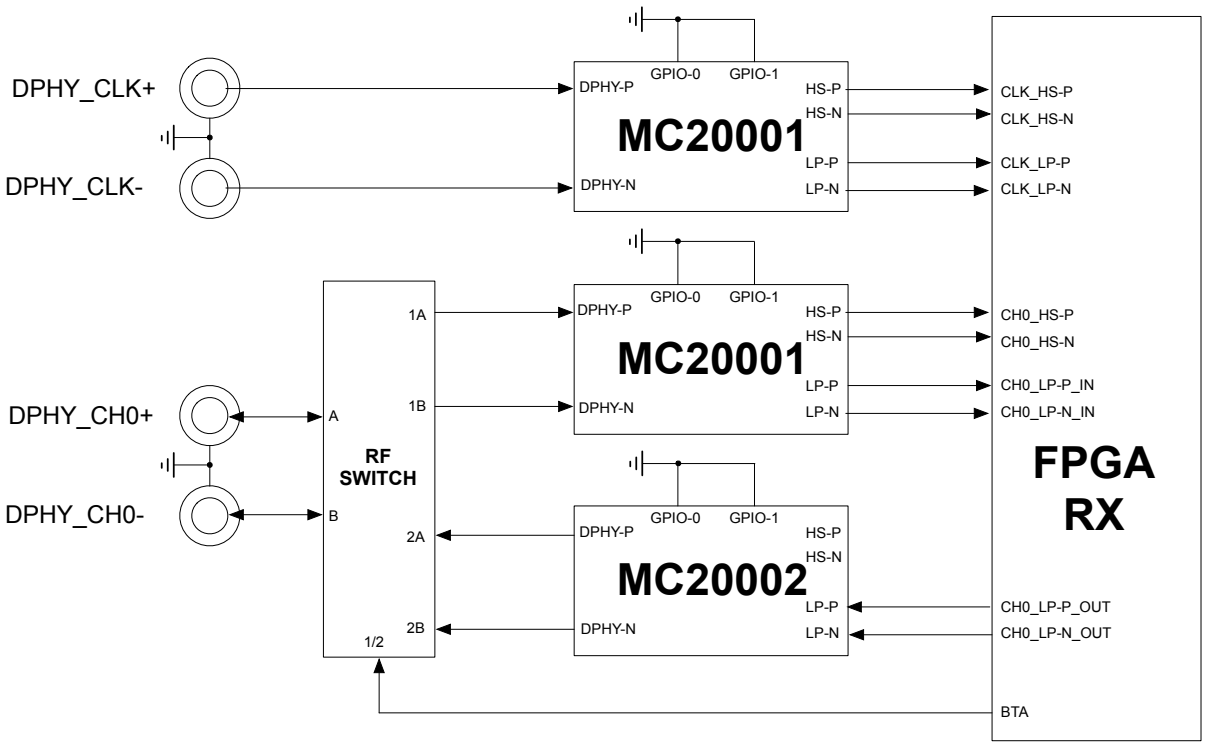


Figure 7: D-PHY to FPGA Bridge Application with Bus Turnaround

6.4 Signal Levels

6.4.1 HS-P and HS-N LVDS Outputs

The common mode voltage is the same as V_{DD}. The differential swing is typically 300mV.

6.4.2 LP-P and LP-N CMOS Outputs

MC20001 generates a 'High' level logic output voltage the same as V_{DDIO}.

6.4.3 DPHY-P and DPHY-N Inputs

These signals are compliant with the MIPI D-PHY specification.

6.5 Configuration Using GPIO-0 and GPIO-1

GPIO-1	GPIO-0	Description
0	0	Accepts D-PHY input
0	1	LP transmission only
1	0	SLVS to LVDS conversion mode activated
1	1	IC power down

Table 6: GPIO Selection Bits

6.6 Input to Output Signal Diagram

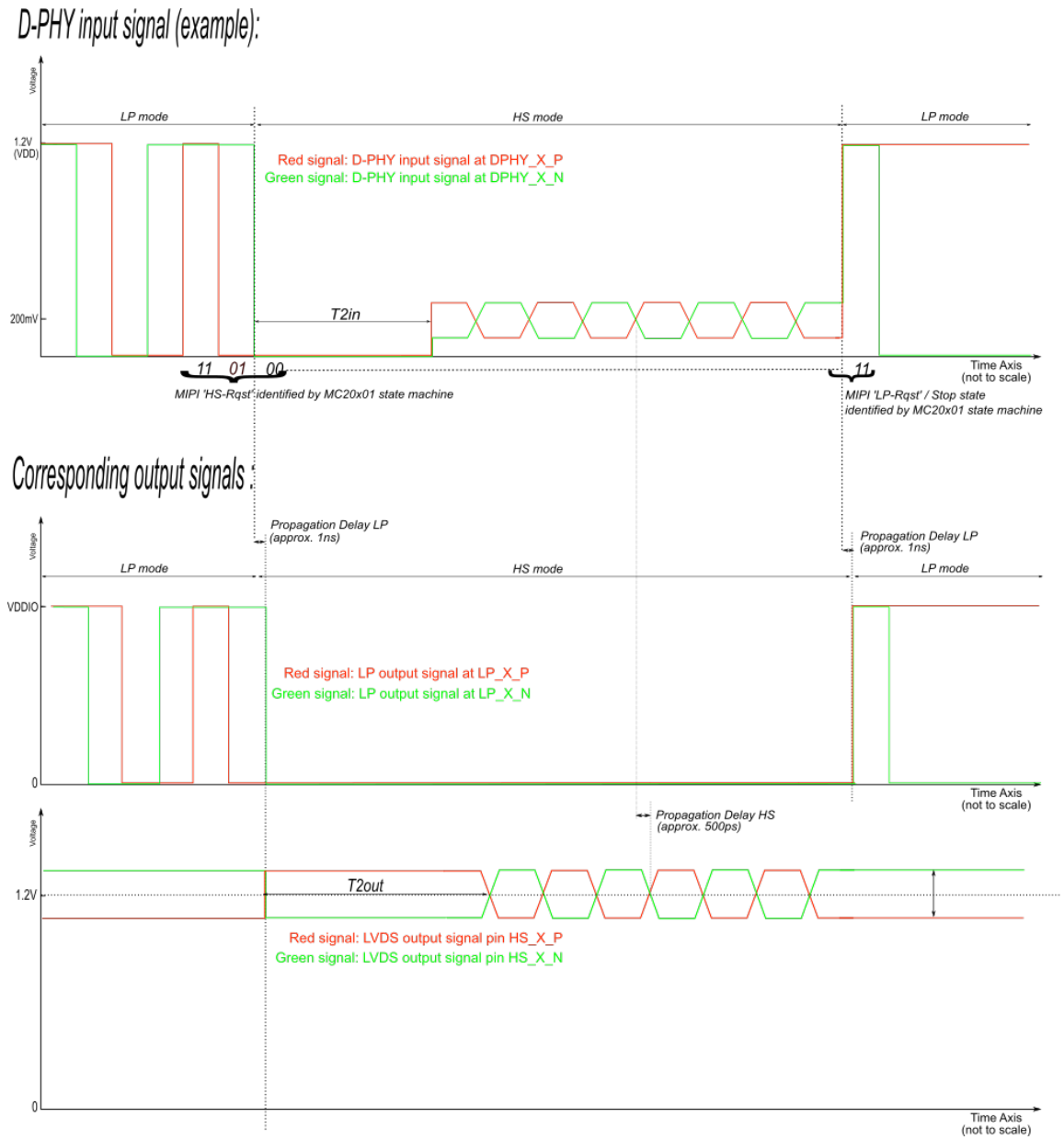


Figure 8: Input to Output Signal Diagram

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